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06CS33

Third Semester B.E. Degree Examination, June/July 2013
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Why NAND and NOR gates are universal gates? Simplify the following Boolean expression using k – map and implement the same using
i) NAND gates only (SOP form)
ii) NOR gates only (POS form)
$F(A, B C,D) = \Sigma_m (0, 1, 2, 4, 5, 12,14) + dc(8, 10)$. **(10 Marks)**

b. Find the prime implicants and essential prime implicants for the following Boolean expression using Quine McClusky's method.
$F(A, B, C, D) = \Sigma'_m(1, 3, 6, 7, 9, 10, 12, 13, 14, 15)$. **(10 Marks)**

2 a. Realize the Boolean expression
$F(A, B, C, D) = \Sigma'_m = (2, 3, 4, 5, 13, 15) + dc(8, 9, 10, 11)$ using 8 : 1 multiplexers and external gates. **(08 Marks)**

b. Generate the Boolean expression for
$Y_0 = A' B'$, $y_1 = ABC$, $y_2 = AB$, $y_3 = AB' C$ using PROM. **(08 Marks)**

c. Write the HDL code for full adder. **(04 Marks)**

3 a. Design a 2 – bit carry look ahead adder and explain, with an example. **(10 Marks)**

b. Draw the block diagram of 4 – bit adder/ subtractor circuit using full adder and explain the same. **(05 Marks)**

c. Compute the sum in each of the following :
i) $7_8 + 3_8$
ii) $8_{16} + F_{16}$. **(05 Marks)**

4 a. What is a fliplfop? Explain the different types of flipflops along with truth table, circuit diagram, and excitation table. **(10 Marks)**

b. Convert the SR flipflop into JK and D flipflops. **(06 Marks)**

c. Write a note on edge trigged flipflps. **(04 Marks)**

PART – B

5 a. What is a register? Explain the types of register along with their applications. **(10 Marks)**

b. Design a synchronous mod- 5 counter using JK flipflop. **(05 Marks)**

c. What are presettable counters? Explain with an example. **(05 Marks)**

6 a. Differentiate Mealy and Moore models. **(05 Marks)**

b. Design an asynchronous sequential logic circuit for the following state transition diagram. **(05 Marks)**

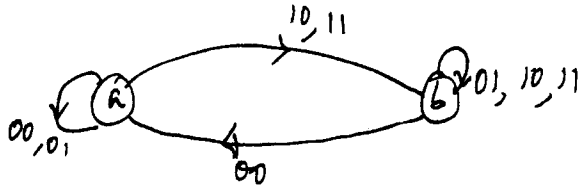

Fig. Q6(b)

c. Draw the state transition diagram by row elimination method for the following :

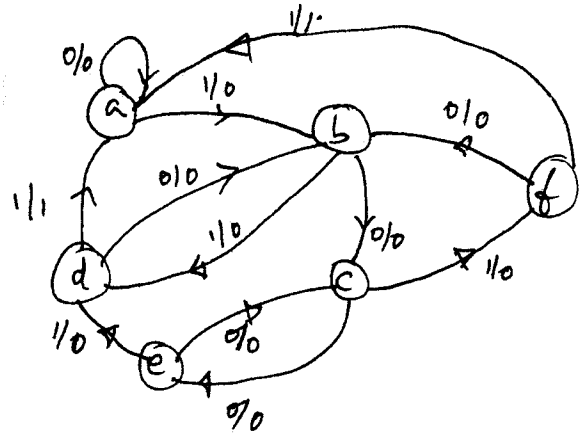

Fig. Q6(c)

(10 Marks)

7 a. Draw and explain the 4-bit binary ladder D/A converter. **(10 Marks)**

b. Discuss any two methods of A/D conversim. **(10 Marks)**

8 a. Define : i) TTL parameters ii) Open – collector gate. **(05 Marks)**

b. What are CMOS characteristics? Explain. **(05 Marks)**

c. With the aid of a circuit diagram, explain the operation of a 2 – input TTL NAND gate with an open – collector method. **(10 Marks)**

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